WHAT IS CLAIMED IS:

1. Clock control circuitry for selectively applying a clock signal to a digital processing component, said clock signal capable of being changed to a plurality of operating frequencies, said clock control circuitry operable to (i) receive a command to change a first operating frequency to a second operating frequency, (ii) in response to said command, disable said applied clock signal, (iii) generate a test clock signal having said second operating frequency, (iv) apply said test clock signal to a power supply adjustment circuit, and (v) sense a status signal from said power supply adjustment circuit indicating that a power supply level of said digital processing component has been adjusted to an optimum value suitable for said second operating frequency.

2. The clock control circuitry for selectively applying a clock signal to a digital processing component as set forth in Claim 1 wherein said clock control circuitry is further operable in response to said status signal to set said applied clock signal to said second operating frequency.

3. The clock control circuitry for selectively applying a clock signal to a digital processing component as set forth in Claim 2 wherein said clock control circuitry is further operable to enable said applied clock signal.

4. The clock control circuitry for selectively applying a clock signal to a digital processing component as set forth in Claim 1 further comprising clock divider circuitry and a controller.

5. The clock control circuitry for selectively applying a clock signal to a digital processing component as set forth in Claim 4 wherein said controller is operable to disable said applied clock signal in response to said received command and enable said applied clock signal in response to said status signal.

6. The clock control circuitry for selectively applying a clock signal to a digital processing component as set forth in Claim 4 wherein said clock divider circuitry is operable to generate said test clock signal having said second operating frequency.

7. The clock control circuitry for selectively applying a clock signal to a digital processing component as set forth in Claim 1 further operable to set said applied clock signal to said second operating frequency as a function of said test clock signal and said status signal.

8. A method of operating clock control circuitry for selectively applying a clock signal to a digital processing component, said clock signal capable of being changed to a plurality of operating frequencies, said method of operating said clock control circuitry comprising the steps of:

receiving a command to change a first operating frequency to a second operating frequency;

disabling, in response to said command, said applied clock signal;

generating a test clock signal having said second operating frequency;

applying said test clock signal to a power supply adjustment circuit; and

sensing a status signal from said power supply adjustment circuit indicating that a power supply level of said digital processing component has been adjusted to an optimum value suitable for said second operating frequency.

9. The method of operating clock control circuitry for selectively applying a clock signal to a digital processing component as set forth in Claim 8 further comprising the step of setting, in response to said status signal, said applied clock signal to said second operating frequency.

10. The method of operating clock control circuitry for selectively applying a clock signal to a digital processing component as set forth in Claim 9 further comprising the step of enabling said applied clock signal.

11. The method of operating clock control circuitry for selectively applying a clock signal to a digital processing component as set forth in Claim 8 wherein said clock control circuitry comprises clock divider circuitry and a controller.

12. A digital circuit comprising:

a digital processing component capable of operating at different clock frequencies;

an adjustable power supply capable of supplying a variable power supply level, VDD, to said digital processing component;

power supply adjustment circuitry capable of adjusting VDD; and

clock control circuitry for selectively applying a clock signal to said digital processing component, said clock signal capable of being changed to a plurality of operating frequencies, said clock control circuitry operable to (i) receive a command to change a first operating frequency to a second operating frequency, (ii) in response to said command, disable said applied clock signal, (iii) generate a test clock signal having said second operating frequency, (iv) apply said test clock signal to said power supply adjustment circuit, and (v) sense a status signal from said power supply adjustment circuit indicating that a power supply level of said digital processing component has been adjusted to an optimum value suitable for said second operating frequency.

13. The digital circuit as set forth in Claim 12 wherein said clock control circuitry is further operable in response to said status signal to set said applied clock signal to said second operating frequency.

14. The digital circuit as set forth in Claim 13 wherein said clock control circuitry is further operable to enable said applied clock signal.

15. The digital circuit as set forth in Claim 12 wherein said clock control circuitry further comprises clock divider circuitry and a controller.

16. The digital circuit as set forth in Claim 15 wherein said controller is operable to disable said applied clock signal in response to said received command and enable said applied clock signal in response to said status signal.

17. The digital circuit as set forth in Claim 15 wherein said clock divider circuitry is operable to generate said test clock signal having said second operating frequency.

18. The digital circuit as set forth in Claim 12 wherein said clock control circuitry is further operable to set said applied clock signal to said second operating frequency as a function of said test clock signal and said status signal.

19. The digital circuit as set forth in Claim 12 further comprising N delay cells coupled in series, each of said N delay cells having a delay D determined by a value of VDD, such that a clock edge applied to an input of a first delay cell ripples sequentially through said N delay cells.

20. The digital circuit as set forth in Claim 19 wherein said power supply adjustment circuitry is operable to (i) monitor outputs of at least a K delay cell and a K+1 delay cell, (ii) determine that said clock edge has reached an output of said K delay cell and has not reached an output of said K+1 delay cell, and (iii) generate a control signal capable of adjusting VDD.

21. The digital circuit as set forth in Claim 20 wherein said power supply adjustment circuitry is further operable to determine that said clock edge has reached said K delay cell output and has not reached said K+1 delay cell output when a next sequential clock edge is applied to said first delay cell input.

22. The digital circuit as set forth in Claim 21 wherein a total delay from said first delay cell input to said K delay cell output is greater than a maximum delay of said digital processing component.